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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/732,700	12/11/2000	Shinya Udo	024014-00001	2922

7590 11/07/2003

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 600
Washington, DC 20036-5339

EXAMINER

ANYASO, UCHENDU O

ART UNIT	PAPER NUMBER
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2675

DATE MAILED: 11/07/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/732,700

Applicant(s)

UDO ET AL.

Examiner

Uchendu O Anyaso

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. **Claims 1-11** are pending in this action.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 1-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Takita et al* (U.S. 6,151,005) in view of Yanagi et al (U.S. 6,310,616), and further in view of *Johnson* (U.S. 5,625,373).

Regarding **independent claim 1**, and for **claim 11**, Takita teaches an X-driver circuit (100) which delivers a voltage corresponding to the display data to each data line of the liquid crystal panel (column 5, lines 25-34, figures 1, 2 at 100).

Furthermore, Takita teaches a grayscale voltage generating portion by teaching voltage divider circuits (120-0, 206) by which a voltage across the outputs (204, 205) is divided into voltages of 16 levels (column 11, lines 44-60, figure 2 at 120-0, 204-206; *see also* column 12, lines 14-37, figure 2 at 120-0, 204-206).

Also, Takita teaches a selector portion for each of the data bus lines and selecting any one of the plurality of analog grayscale voltages based on the grayscale data by teaching an X driver circuit into which display data to be displayed on a liquid-crystal panel is supplied, and which delivers a voltage corresponding to the display data to each data line of the liquid-crystal panel;

Art Unit: 2675

may well comprise a voltage divider circuit provided for each data line, by which n voltages externally supplied are divided into m voltages ($n < m$) corresponding to the display data; the voltage divider circuit including a first selector circuit which is supplied with the n unequal voltages, and which selects and delivers two of the supplied n voltages; a first control circuit which controls the first selector circuit in accordance with the display data so as to select the two voltages; an output circuit which can deliver either of a plurality of divisional voltages produced from the selected voltages, and the supplied voltages; a second selector circuit which selects and delivers any of the plurality of divisional voltages and the supplied voltages; and a second control circuit which controls the second selector circuit under either of a voltage selection command externally supplied and a voltage selection command internally generated, so as to select the voltage to-be-delivered from either of the supplied voltages and the plurality of divisional voltages corresponding to the display data; the voltage selection command being a command for selecting a higher one of the two voltages selected by the first selector circuit, during a first period, while it is a command for selecting the divisional voltage corresponding to the display data, during a second period subsequent to the first period. (column 5, lines 25-52).

Furthermore, Takita teaches a plurality of grayscale voltages connected to the grayscale (V0-V4) that supplies the grayscale voltages to the selector portion (201) (figure 2 at V0-V4, 201).

However, Takita does not teach a switching portion for electrically connecting and disconnecting a plurality of grayscale voltage lines from a grayscale voltage generating portion. On the other hand, Yanagi teaches a drive circuit for a display device that supplies a plurality of grayscale voltages to the display device (*see* Abstract) comprising capacitors (C1, C2) and

Art Unit: 2675

switching portions (SW₁₁, SW₁₂, SW₂₁, SW₂₂) that enable connecting and disconnecting a plurality of grayscale voltage lines from a grayscale voltage generating circuit P4 (column 38, lines 21-54, figure 31 at 12a, 12b, C₁, C₂, SW₁₁, SW₁₂, SW₂₁, SW₂₂).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Takita and Yanagi's inventions because while Takita teaches an X-driver circuit (100) which delivers a voltage corresponding to the display data to each data line of the liquid crystal panel (column 5, lines 25-34, figures 1, 2 at 100) with switching portions (202, 203) that delivers high and low potentials on the output bus (column 11, lines 63-67 through column 12, lines 1-2, figure 2 at 202, 203), Yanagi teaches capacitors and switching portions for electrically connecting and disconnecting a plurality of grayscale voltage lines from a grayscale voltage generating portion P4 (*see* column 38, lines 21-54, figure 31 at 12a, 12b, C₁, C₂, SW₁₁-SW₂₂; *see also* column 15, lines 20-36). The motivation for combining these inventions would have been to design a high-grade display device with low power consumption (column 16, lines 17-27).

However, Takita and Yanagi do not teach how these switching circuits are used during an operation test. On the other hand, Johnson teaches an invention for conducting operation tests in a flat panel display in order to eliminate visual anomalies wherein an error measurement device (22) is connected to a selector switch (12) that provides electrical connection to each column driver (column 3, lines 55-67; column 7, lines 24-30, figures 3, 6 at 12, 22).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Takita, Yanagi, and Johnson because while the combination of Takita and Yanagi teach a display device that supplies a plurality of grayscale voltages to the display device comprising capacitors and switching portions that enable connecting and disconnecting a plurality of grayscale voltage

Art Unit: 2675

lines from a grayscale voltage generating circuit P4, Johnson teaches an invention for conducting operation tests in a display device in order to eliminate visual anomalies wherein an error measurement device (22) is connected to a selector switch (12) that provides electrical connection to each column driver (column 3, lines 55-67; column 7, lines 24-30, figures 3, 6 at 12, 22). The motivation for combining these inventions would have been to eliminate any sought of visual anomalies that may appear in a display system (column 1, lines 4-6).

Regarding **claims 2 and 3**, in further discussion of claim 1, Takita teaches a voltage generating portion (206) that has a ladder resistor portion with a plurality of resistors connected in series and which generates a plurality of analog grayscale voltages through resistance divisions (figure 2 at 206).

Regarding **claims 4-8**, in further discussion of claim 1, Takita teaches switching portions (202, 203) that delivers high and low potentials on the output bus (column 11, lines 63-67 through column 12, lines 1-2, figure 2 at 202, 203).

Regarding **claims 9 and 10**, in further discussion of claim 4, Johnson teaches an invention for conducting operation tests in a flat panel display in order to eliminate visual anomalies wherein an error measurement device (22) is connected to a selector switch (12) that provides electrical connection to each column driver (column 3, lines 55-67; column 7, lines 24-30, figures 3, 6 at 12, 22).

Art Unit: 2675

Response to Arguments

4. Applicant's submissions i.e., amendments and arguments filed on October 27, 2003 concerning Applicant's Request for Continued Examination with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

In response to all of applicant's arguments, please see rejection above.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,172,663 to *Okada et al* for a driver circuit.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Application/Control Number: 09/732,700

Page 7


Art Unit: 2675

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

10/31/2003



STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600